Abstract of Disclose

A self refresh control device, for use in a semiconductor memory device, comprises a self refresh entry unit having at least one clock buffer for generating a self refresh entry signal in response to an external control signal, wherein the clock buffer generates a clock signal in response to an external clock signal and a clock buffer enable signal; a self refresh exit unit for generating a first self refresh exit signal in response to the external control signal and generating a second self refresh exit signal synchronized with the clock signal; a clock buffer controller for generating the clock buffer enable signal in response to the first self refresh exit signal; and a self refresh signal generator for generating a self refresh signal in response to the self refresh entry signal and the second self refresh exit signal.